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Simulation design and analysis 9-level H-bridge single phase stepdown cyclo inverter

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ABSTRACT

This DC-to-AC voltage converter is designed for output frequency controlled by a 9-level cascade H-bridge cyclo inverter with pulse width adjustment. The aim of the study was to determine the pattern and format of the voltage, output frequency, and Total Harmonic Distortion index of a 9-level IGBT cyclo inverter. The method used is to build a unidirectional power converter design modeling into 9 alternating levels with cyclo converter-controlled frequency settings using the Simulink MATLAB tool. The cyclo converter section is constructed with two P and N converters in a parallel arrangement. The frequency and trigger pulse width of both converters control the output voltage and frequency format of the cyclo inverter. The test results show a series of ladder waves with an output frequency, f_0 of (1/2f, 1/3f, 1/4f, 1/5f, 1/6f, 1/7f, 1/8f, 1/9f, and 1/10f). The simulation results show that the nth input frequency divider waveform is characterized by the emergence of a number of step pulses of n positive half cycles and negative half cycles. The Total Harmonic Distortion Index gets bigger when the system circuit is designed at a low frequency. This modeling can be implemented into a prototype that is used for variable-speed DC motor drivers.

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1. INTRODUCTION

AC to DC converter, better known as an inverter, is a type of power electronics circuit that has been widely used in the community. Its presence is mostly required for control of power equipment. In general, inverters have a square-shaped output wave format, so by engineering the input DC voltage from several levels, the output shape will resemble a sinusoidal wave. This concept is more popular with the multilevel inverter method (MLI). The H-bridge multilevel inverter is an appropriate alternative solution choice among the existing multilevel inverter topologies [1]. This multilevel inverter is generally used as a three-phase induction motor rotational speed controller that requires v/f adjustment using a pulse width setting (PWM) technique [2]. The more the number of levels, the MLI output waveform is closer to the sinusoid so that it will decrease the THD. However, this increase in voltage level is accompanied by disadvantages, among others, that this inverter requires a larger number of switches, a more complicated control system, and a higher cost [3]. MLI can be built using a combination of power semiconductor devices such as MOSFET, and IGBT where the MLI voltage format is in the form of a step-step voltage wave pattern resulting from a predetermined gate switch sequence setting [4], [5]. IGBT is a semiconductor device that is often used in cycloconverter circuits in high-speed and high-frequency induction motor control operations [6]. The inverter voltage source can be a battery, solar power, or other DC voltage source. The multistage inverter is composed of several single-phase H-Bridge inverters

connected in series [7], [8]. MLI is very suitable for high voltage applications, because it has high efficiency, better power quality, small switching losses, decreased magnetic interference, and close to one power factor.

However, it is rather difficult to operate in quadrant 4 in the energy conversion process and the H-bridge inverter can cause voltage spikes on the output side [9]–[11] so that the MLI still contains harmonic components on the output side of the waveform in the form of non-sinusoidal. In low-power applications, this non-sinusoidal voltage spike can still be tolerated, but for high-power applications, the presence of harmonics is a serious problem that requires handling [12]. Important things to consider in designing an MLI are the use of a minimum number of switches and a DC source voltage, a simple drive circuit, and low cost. Inverter output voltage regulation can be done using PWM control. This method is very efficient and effective where the DC source voltage is fixed while the output voltage is regulated through the ON-OFF period of the inverter switch [13]. There are three basic topologies for multilevel inverters, including diode clamped MLI, flying capacitors MLI, and cascaded H-bridge MLI [14]. Inverter classification can also be categorized into two types, namely inverters with symmetrical and non-symmetrical topologies. The first type of topology has an identical source voltage level while the non-symmetrical type has a voltage input with different amplitude, number of switches, and switching sequences so that the topological modularity remains incomplete [15], [16]. On the other hand, harmonic disturbances can occur in the power system when the first AC system is created [17]. The trigger angle of the inverter switch gate requires precise considerations and calculations so that a small THD index can be obtained. There are various kinds of control for inverters, one of the simplest control methods is sinusoidal pulse width modulation (SPWM) [18], [19]. The SPWM-based method is the right way to reduce THD in a multilevel inverter gate switch because it has a better dynamic response and small commutation load with reduced switching losses [20] .Some other applications of this inverter are to control the speed regulation of induction motors [21] and as an intermediary in the power grid between renewable electrical energy (PV) generators and power plants [22]. Cyclo inverter is another type of power electronics circuit that has a working pattern of converting fixed frequency AC power into variable frequency AC power format [23] the output frequency of the cyclo converter can be greater or less than the input frequency [24]. The cyclo converter consists of converter P and converter N arranged in parallel. The frequency of the output waveform can be adjusted by varying the number of cycles of the converter P in the positive period and the converter N in the negative cycle. The number of cycle variations as an integer multiple of the input frequency. Cyclo inverter is widely used as an induction motor drive from small to a large power.

Research related to cyclo inverters is still rarely done. The author only found a few articles but the most recent one was about four years ago. So that this research needs to be developed in order to find new discoveries. Several previous researchers, including Mayank Kumar, made a soft switch for a single-phase cyclo inverter switch based on IGBT which resulted in a change in the input frequency voltage into an output voltage at a high frequency to improve device performance compared to the use of PWM [25]. Sudhin Govind engineered a cyclo inverter for controlling a high-power single-phase induction motor using an IGBT semiconductor switch where the output is an integer multiple of the input frequency. This paper describes the development of a single-phase cyclo inverter by inserting 9-levels of IGBT H-bridge Inverter through modeling simulation using the Simulink MATLAB tool.

2. METHOD

This research work was carried out through several stages. The workflow is shown in Figure 1. Figure 1 is the flow of the research method that is being carried out. The first step is to collect literature from various library sources to deepen knowledge related to cyclo inverters. The second stage is to design the concept of a 9-level cascade H-bridge and a cyclo inverter using an IGBT semiconductor device with an input voltage of 9 volt for each step electronically. The next step is to build an electronic design modeling design into the MATLAB/Simulink tool accompanied by a model of the trigger pulse generator circuit for the two circuits. The next stage is testing and observing a circuit of models by running the model on a MATLAB application. The test results were then analyzed and compared with the literature and concluded as the last step.

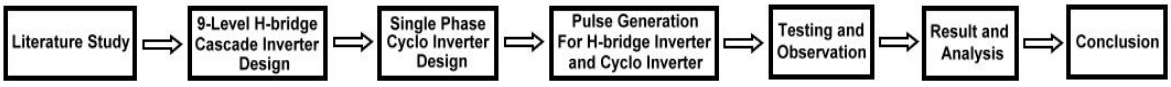


Figure 1. System design research flow

Figure 2 is an electronic system design and there are four main parts. The first part is the design of a 9-level IGBT switch using 4 cascade H-bridge inverter bridges arranged in series. Each hybrid inverter is supplied with the same DC voltage of 48 volts separately. The basic idea is to convert different DC input

voltage levels into AC voltages. The number of bridge inverters can be determined by (*m*-1)/2 where m is the number of inverter levels. Each inverter bridge circuit has an output voltage of $+V_{DC}$, 0, and $-V_{DC}$. Thus, the maximum output voltage value is 9×48 Vpp (volts peak to peak). The performance of each H-bridge inverter can be regulated by the gate pulse on each switch. The second part is a cyclo converter circuit consisting of a P (Positive) converter and an N (Negative) converter which is connected in parallel with the load. The P converter is an arrangement of bridge rectifiers using silicon-controlled rectifier (SCR) to carry the input current in the positive cycle, while the N converter consists of a bridge rectifier circuit in the opposite direction to the P converter. This N converter plays a role in flowing input current in the negative cycle. The pattern and waveform of the output current depending on the pulse settings on each switch of the P converter and the N converter. The trigger pulse of the P converter and N converter will change the input frequency of the 9-level inverter to a lower and varied frequency. The third and fourth parts are the trigger pulse generator for 9-level inverter performance with a pulse width modulation (PWM) pulse generator while the cyclo converter circuit trigger pulse uses a pulse width setting.

Figure 3 is a modeling system from Figure 2 using MATLAB/Simulink tools. The bridge circuit is arranged in series with the input voltage of each switch of 48 volts. The switch of each bridge has four trigger gates (G1-G4) first level, (G5-G8) second level, (G9-G12) third level, and (G13-G16) in the fourth level.

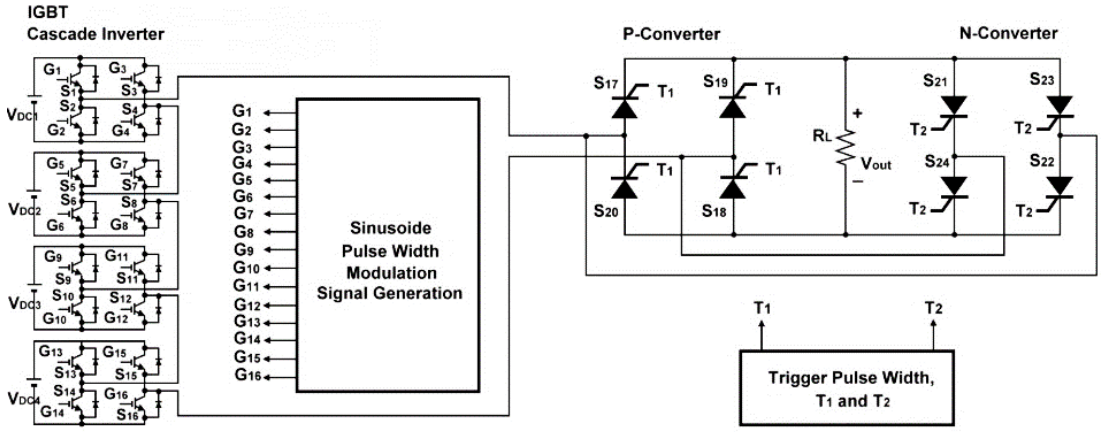


Figure 2. Electronic design 9-levels IGBT cascade H-bridge cyclo inverter

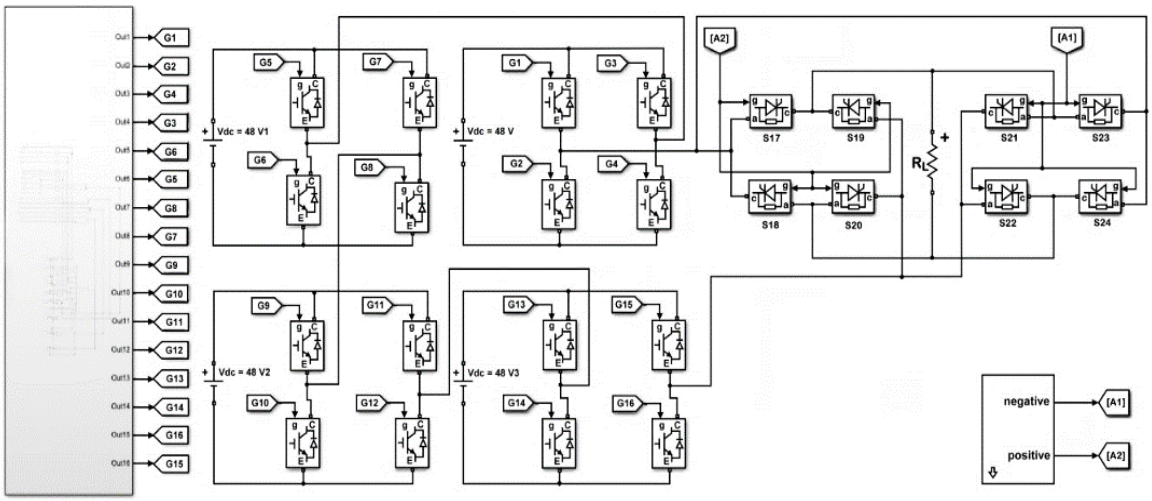


Figure 3. Cyclo inverter 9-level modeling

3. RESULTS AND DISCUSSION

In this section, it is explained the results of the research and at the same time is given the comprehensive discussion. Results can be presented in figures, graphs, tables, and others that make the reader understands easily. The discussion can be made in several sub-sections.

3.1. 9-level inverter gate trigger pulse generator

The inverter's 9-level switch cascade performance is activated by PWM pulses. There are two kinds of PWM pulse width modulation techniques, namely phase shifted PWM (PS PWM) and level-shifted PWM (LS PWM). PS PWM uses several triangular carrier signals that have the same amplitude and frequency but there is a phase shift between the carrier waves. The number of carrier signals with *n* levels required is (*n*-1). While the phase shift can be determined at (360^0/n-1). The PWM gate pulses are obtained from the proper comparison of the carrier signal and the triangular signal as well as the modulating signal. Level-Shifted PWM (LS PWM) also requires a number of triangular carrier signals but is applied at different levels. This type of modulation produces a smaller THD.

Figure 4 is an LS PWM pulse generator by modulating a sinusoidal signal on a triangular carrier signal with a frequency of 200 Hz. There are 16 gate switch inverters (G1-G16) that must be activated with a gate pulse so that it requires 8 (eight) triangular carrier waves at the same amplitude and frequency but the carrier signals are set at different levels. Using a sinusoidal wave comparator compared to the carrier signal will produce an output wave pulse with a PWM-controlled pulse width. The inverting circuit is mounted on the output side so that two pulse signal patterns of opposite levels are obtained to activate the switch pair. In the Simulink application, the sequence of the carrier waves for each pulse generator for switching on is declared as the time value and output value. The time value of all carriers is set to the same value, namely 0 2.5e-3 5e-3. The output value can be seen in Table 1. Table 1 lists the repeating sequence carrier waveform levels used to generate PWM pulses for the four H-bridge switches. The results of the pulses generated are shown in Figure 5.

Figure 5 is a series of 9-level inverter gate switching pulses G1 – G16. The pulse has an amplitude of 1 volt, and a frequency of 200 Hz, with the pulse width for each switch varying. The switch pairs of each inverter level are triggered by pulses that are complementary or opposite logic. For example, in pair G1 and G2, when switch S1 is triggered by pulse G1 logic high (1) then switch S2 is activated with pulse G2 in logic low (0). And so on for the G3 and G4, G5 and G6 pairs, and other switch pairs.

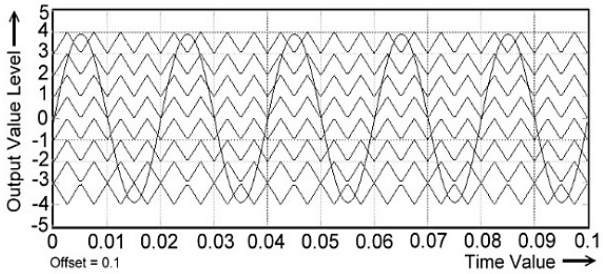


Figure 4. LS PWM Sinusoidal modulation and triangular carrier signal

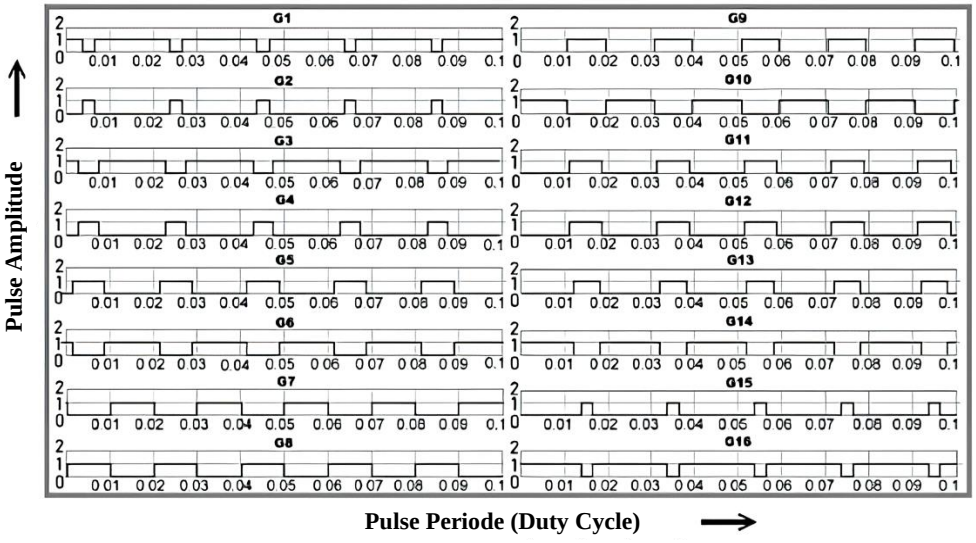


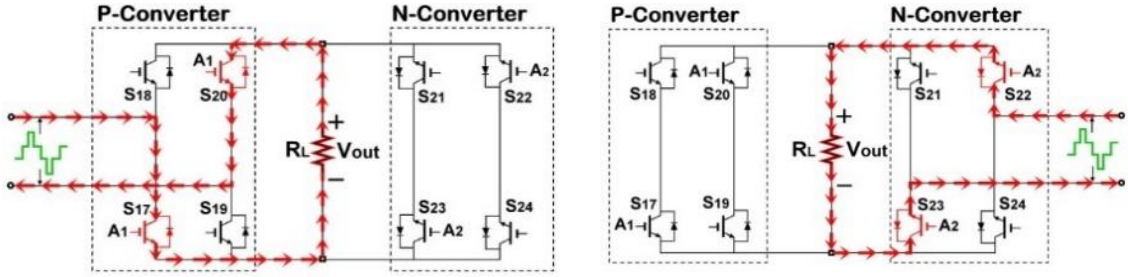
Figure 5. LS PWM trigger pulse for G1–G16

Table 1. PWM pulse generation carrier wave level

Number of Carrier Signal	Time Value	Output Value Level	Firing Switch Gate
1	0 2.5e-3 5e-3	3 4 3	G1 and G2+NOT Gate
2	0 2.5e-3 5e-3	2 3 2	G3 and G4 + NOT Gate
3	0 2.5e-3 5e-3	1 2 1	G5 and G6 + NOT Gate
4	0 2.5e-3 5e-3	0 1 0	G7 and G8 +NOT Gate
5	0 2.5e-3 5e-3	-1 0 -1	G9 and G10+NOT Gate
6	0 2.5e-3 5e-3	-2 -1 -2	G11 and G12+NOT Gate
7	0 2.5e-3 5e-3	-3 -2 -3	G13 and G14 +NOT Gate
8	0 2.5e-3 5e-3	-3 -4 -3	G15 and G16 + NOT Gate

3.2. Gate trigger pulse generator and cyclo inverter switch performance

Generally, a cyclo inverter converts a sinusoidal input with a fixed frequency into an AC wave with a variable frequency. However, in this study, the cyclo inverter circuit gets input in the form of a ladder voltage that comes from the output voltage of the IGBT 9-level inverter unit. The inverter functions as a controlled bridge rectifier. The P inverter operates in the positive half-cycle rectifier process and the N inverter acts to flow current in the negative half-cycle. The bridging switch on the cyclo inverter P (S17, S18, S19, S20) inverter circuit is triggered using an A1 trigger pulse while on the N inverter (S21, S22, S23, S24) it is activated with A2 pulses. There are two modes of cyclo inverter performance, namely the mode when the P inverter is ON then the inverter N is OFF and the second mode is when the N inverter turns ON and the P inverter turns OFF. As shown in Figure 6(a), the working principle is when the cyclo inverter gets a positive cycle input voltage from a 9-level voltage source, current flows through the switch S17, the load RL, S20 then returns to the source (in according to arrowed dash line). The S18 switch is useful for blocking the input current from being connected directly to the P inverter and diverting the input current to pass through the S17 switch. While switch S19 is needed to block the current from switch S17 so that it does not go to the source because a short circuit will occur, but the current has flowed to the load and back to the source. So, on Figure 6(b) when working on a negative cycle, the input current will flow through S22, Load RL, S23, and back to the source. S24 is used to block the flow of current from S22 so that it does not return directly to the source but is transferred to the load and then through S23 the current returns to the source.



(a) (b)

Figure 6. Power flow of cyclo inverter on (a) positive mode (b) negative mode

Figure 7 describes two signals A1 and A2 which are used to activate the inverter P and inverter N. The gate signal has a phase difference of 180^0 with an amplitude of 1 volt set at a frequency multiple of 1/n of the input frequency of 50 Hz. Table 2 shows the timing of the trigger signal periods A1 and A2 for each 1/n divider of the cyclo inverter.

Figure 8 explains the output voltage pattern of a 9-level inverter consisting of four voltage levels at the positive cycle level (V1, V1+V2, V1+V2+V3, V1+V2+V3+V4), zero level, and four levels in the negative cycle. (-V1, -V1-V2, -V1-V2-V3, -V1-V2-V3-V4). Positive level voltage `'V', switches S1, S4, S5, S7, S9, S11, S13 and S15 always turn on in the ON state (1 = ON, 0 = OFF). Likewise, to generate a voltage at the negative level '-V', switches S2, S3, S6, S8, S10, S12, S14 and S16 are always turned on in the ON state. In the positive cycle (V_p) the value of the voltage V_1, V_2, V_3, V_4 can be determined by the following in (1):

$$
\begin{aligned}
V_1 &= A[u(t-t_1) - u(t-t_8)] \\
V_2 &= 2A[u(t-t_2) - u(t-t_7)] \\
V_3 &= 3A[u(t-t_3) - u(t-t_6)] \\
V_4 &= 4A[u(t-t_4) - u(t-t_5)] \\
V_p &= (V_1 + V_2 + V_3 + V_4)
\end{aligned} \tag{1}
$$

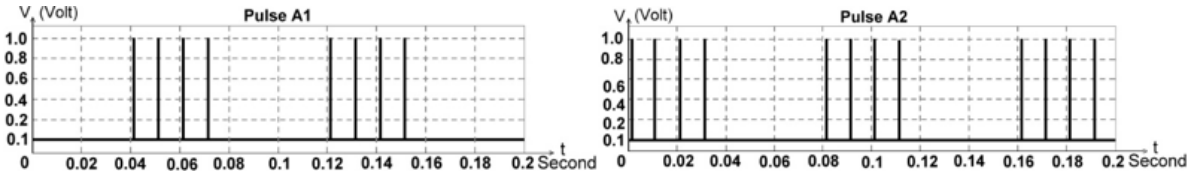


Figure 7. Cyclo inverter circuit trigger signal of A1 and A2

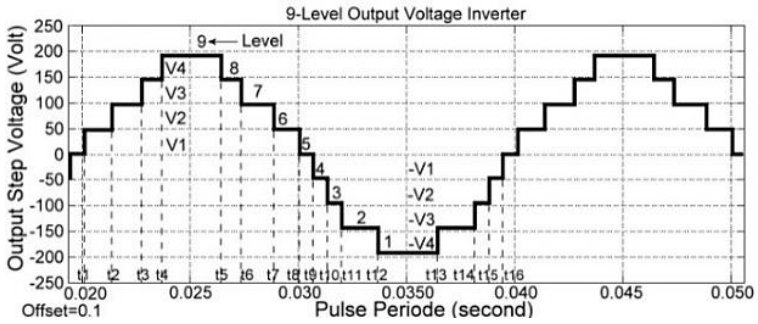


Figure 8. Output voltage form 9-Level H-bridge inverter

Table 2. Period, V_{rms} and THD at each frequency of the cyclo inverter output voltage

Divisor to	Pulse Periode A1 and A2 (s)	Fout (Hz)	Vrms (V)	THD (%)
1	0.02	50	130,62	14.33
½	0.04	25	110,52	65,64
1/3	0.06	16,667	106,27	73.72
¼	0.08	12.5	105.41	75.47
1/5	0.1	10	104.68	76.88
1/6	0.12	8.333	104.56	77.34
1/7	0.14	7.142	104.28	77.48
1/8	0.16	6.25	104.25	77.82
1/9	0.18	5.55	103.97	77.91
1/10	0.2	5	104.03	77.95

In the negative cycle (V_n) the value of the voltage V_5, V_6, V_7, V_8 can be determined by the following in (2).

$$\begin{aligned} V_5 &= -A[u(t-t_9) - u(t-t_{16})] \\ V_2 &= -2A[u(t-t_{10}) - u(t-t_{15})] \\ V_3 &= -3A[u(t-t_{11}) - u(t-t_{14})] \\ V_4 &= -4A[u(t-t_{12}) - u(t-t_{13})] \\ &\dots \\ V_n &= (V_5 + V_6 + V_7 + V_8) \end{aligned} \quad (2)$$

So that in one 9-level ladder wave cycle can be determined by the (3).

$$V_T = (V_p + V_n) \quad (3)$$

The average voltage value of one cycle on n (4).

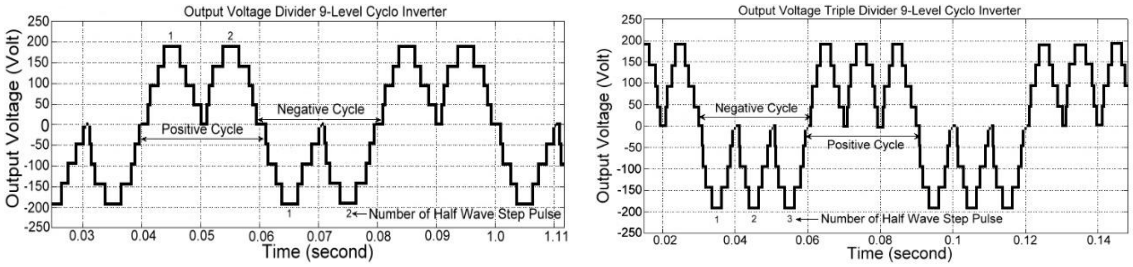
$$V_{avr} = \frac{1}{T}\int_{t_0}^{t_0+T} V_p\, dt + \frac{1}{T}\int_{t_0}^{t_0+T} V_n\, dt) \quad (4)$$

The value of the effective stress (rms) one cycle can be determined by the (5).

$$V_{rms} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} V_p\, dt + \frac{1}{T}\int_{t_0}^{t_0+T} V_n\, dt)} \quad (5)$$

Figure 9(a) is a cyclo inverter divider (divider of two) waveform which has two ladder waves of four levels of a 9-level half-wave cyclo inverter on a positive cycle and two ladder waves of four levels of a half-wave cyclo inverter on a negative cycle. One period (T) of the wave is 0.04 s so that the frequency of the wave ($1/T$) is 25 Hz.

Figure 9(b) describes the same conditions in the cyclo inverter triple divider, the output wave pattern appears three 4-level cyclo inverter half-wave signals in the positive cycle and three 4-level cyclo inverter half-wave signals in the negative cycle. One wave cycle takes $T = 0.06$ ms so that the frequency of the cyclo inverter output waveform can be determined ($1/T$) of 16,667 Hz. Thus, it can be said that for the n-th frequency divider of a cyclo inverter, at the output voltage there will be n integer multiples of the cyclo inverter half-wave signal in the positive cycle and n cyclo inverter half-wave signals in the negative cycle.



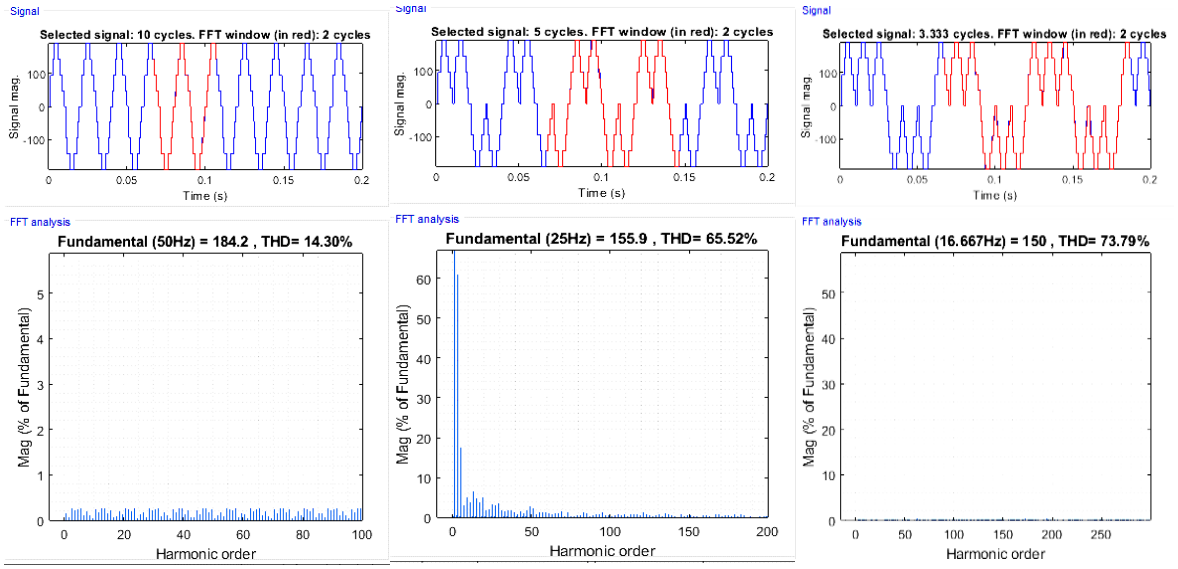
(a) (b)

Figure 9. Cyclo inverter output voltage at a frequency of (a) 25 Hz and (b) 16.667 Hz

Table 3 is the condition of the switch (S1 – S16) when it is at the positive cycle level, level 0 and negative level. The battery voltage for each inverter is 48 volts, so the lowest level is at -192 volts and the highest level is 192 volts. The zero point of the voltage is at level five. The multilevel inverter ladder wave is designed to resemble a sinusoidal wave, but in reality, the wave still has distortion so it is not pure sinusoidal. Figure 10(a) is the THD index value of the 9-level output voltage waveform of 14.33% which states the shift of the output waveform to the sinusoidal shape. Figure 10(b) is the THD index of the voltage divider at a frequency of 25 Hz cyclo inverter of 65.64%. This value is quite high because the resulting waveform is still far from a sinusoidal shape. Figure 10(c) is a cyclo inverter three divisor THD index value of 73.72%. Similar to the previous divisor THD index value, the THD value increases because the output waveform shift does not resemble a sinusoidal waveform. This is because the form factor of the input waveform is not sinusoidal and already contains a large harmonic index. So, to lower the THD index, a filter that is tuned at the right frequency is needed so that the harmonic value is low.

Table 3. Voltage level when cyclo inverter operates on positive cycle and negative cycle

State of Switch	Output Voltage Level (V_0)								
	Negative Cycle				0	Positive Cycle			
	1 (-192 V)	2 (-144 V)	3 (-96 V)	4 (-48 V)	5 (0 V)	6 (48 V)	7 (96 V)	8 (144 V)	9 (192 V)
S1	0	0	0	0	-	1	1	1	1
S2	1	1	1	1	-	0	0	0	0
S3	1	1	1	1	-	0	0	0	0
S4	0	0	0	0	-	1	1	1	1
S5	0	0	0	0	-	1	1	1	1
S6	1	1	1	1	-	0	0	0	0
S7	1	1	1	0	-	1	0	0	0
S8	0	0	0	1	-	0	1	1	1
S9	0	0	0	0	-	1	1	1	1
S10	1	1	1	1	-	0	0	0	0
S11	1	1	0	0	-	1	1	0	0
S12	0	0	1	1	-	0	0	1	1
S13	0	0	0	0	-	1	1	1	0
S14	1	1	1	1	-	0	0	0	1
S15	1	0	0	0	-	1	1	1	0
S16	0	1	1	1	-	0	0	0	1



(a) (b) (c)

Figure 10. THD index value of (a) output voltage 9-level inverter; (b) voltage divider of two cyclo inverter (c) cyclo inverter triple voltage

4. CONCLUSION

A 9-level cyclo inverter can be constructed using 4-multistage inverters connected in series as input voltage sources. The frequency divider circuit is formed by a controlled bridge rectifier circuit which is controlled by a pulse width setting. The pulse width of the controlled rectifier setting determines the frequency and waveform of the cyclo inverter output voltage. The output voltage waveform and pattern of the 9-level cyclo inverter on the nth frequency divider consists of n numbers of 4-level half-wave signals in the positive cycle and n total 4-level half-wave signals in the negative cycle. The THD index of the *n*-th divisor at the frequency decreases to n the greater this is because the shape factor of the output waveform has a large enough shift from the sinusoidal shape. The use of this cyclo inverter circuit is more precisely implemented in DC motor speed regulation because the waveform resembles a DC chopper voltage wave.

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